

Total No. of Questions—8]

[Total No. of Printed Pages—2

Seat No.	
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[5352]-569

S.E. (Computer) (II Sem.) EXAMINATION, 2018

MICROPROCESSOR

(2015 COURSE)

Time : Two Hours

Maximum Marks : 50

- N.B. :—**
- (i) Answer Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4, Q. No. 5 or Q. No. 6, Q. No. 7 or Q. No. 8.
 - (ii) Neat diagram must be drawn whenever necessary.
 - (iii) Figures to the right indicate full marks.
 - (iv) Assume suitable data, if necessary.

1.
 - (a) Explain immediate and register addressing mode with an example. [2]
 - (b) Draw and explain the flag register of 80386. [4]
 - (c) Draw and explain segment descriptor. [6]
- Or*
2.
 - (a) What is the use of Interrupt Flag ? [2]
 - (b) Explain paging mechanism. [4]
 - (c) Draw and explain the 80386 address translation mechanism considering PG bit in CR0 in set. [6]
3.
 - (a) What is CPL and RPL ? [2]
 - (b) Explain Interrupt no. 0 and 4. [4]
 - (c) Explain the role of Task Register in multitasking and the instructions used to modify and read TR. [6]

P.T.O.

Or

4. (a) List five aspects of protection in the 80386. [2]
(b) Write a short note on 'I/O permission Bit Map'. [3]
(c) Draw and explain TSS. [7]

5. (a) Write short note on Virtual 8086 Mode. [3]
(b) Explain software initializations required for protected mode. [4]
(c) Draw and explain structure of the TLB. [6]

Or

6. (a) What are the contents of various registers of processor 80386 after reset ? [3]
(b) Explain entering and leaving V86 mode. [4]
(c) Draw and explain debug registers of the 80386. [6]

7. (a) Explain the following signals : [3]
(i) W/R##
(ii) D/C#
(iii) M/IO#
(b) Explain any *four* 80387 constant instructions. [4]
(c) Draw read cycle with non-pipelined address timing. [6]

Or

8. (a) Explain the following signals : [3]
(i) INTR#
(ii) NMI#
(iii) RESET#
(b) Draw and explain 80387 register stack. [4]
(c) Explain any *six* 80387 data transfer instructions. [6]