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[5668]-189

S.E. (Computer) (Second Semester) EXAMINATION, 2019

MICROPROCESSOR

(2015 PATTERN)

Time : Two Hours

Maximum Marks : 50

N.B. :— (i) Answer question Nos. 1 or 2, 3 or 4, 5 or 6, 7 or 8.

(ii) Neat diagram must be drawn wherever necessary.

(iii) Figures to the right indicate full marks.

(iv) Assume suitable data, if necessary.

1. (a) List and explain coprocessor interface instructions of 80386. [2]
- (b) With the help of diagram explain 80386 applications register set. [4]
- (c) Explain how linear address 0080400A H will be translated into physical address using paging mechanism. Whether the address generated will be the same to linear address ? [6]

Or

2. (a) Explain LEA and XLAT instructions. [2]
- (b) Draw and explain EFLAGS register of 80386. [4]

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- (c) With the help of diagram explain the 80386 mechanism to translate logical address to linear address and linear to physical address. [6]

3. (a) List aspects of protection related to pages. [2]
(b) Write a short note on “Multitasking” feature of 80386. [4]
(c) List different sources of interrupts and explain different ways by which 80386 can enable and disable interrupts. [6]

Or

4. (a) Define DPL, RPL and CPL. [2]
(b) Write a short note on “Task Linking”. [4]
(c) List mechanism which provide protection for I/O functions and explain the role of IOPL in providing protection for I/O functions. [6]
5. (a) Write a short note on “Virtual 8086 mode”. [3]
(b) Explain 80386 processor state after RESET. [4]
(c) What all initializations required to start processor in real mode after reset ? [6]

Or

6. (a) Explain, how test registers are used in testing TLB ? [7]
(b) What all initializations required to start processor in protected mode after reset ? [6]

7. (a) Explain HOLD and HLDA signals of 80386DX. [4]
(b) Draw and explain 80387 register stack. [4]
(c) Draw and explain bus states and transitions when address pipelining is not used. [5]

Or

8. (a) List various bus states when address pipelining is used. [4]
(b) Which data types are supported by 80387 ? [4]
(c) Draw write cycle with non-pipelined address timing. [5]